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#ArmDevSummit

Cloud-based Automated SoC Design for an Intelligent Sensor

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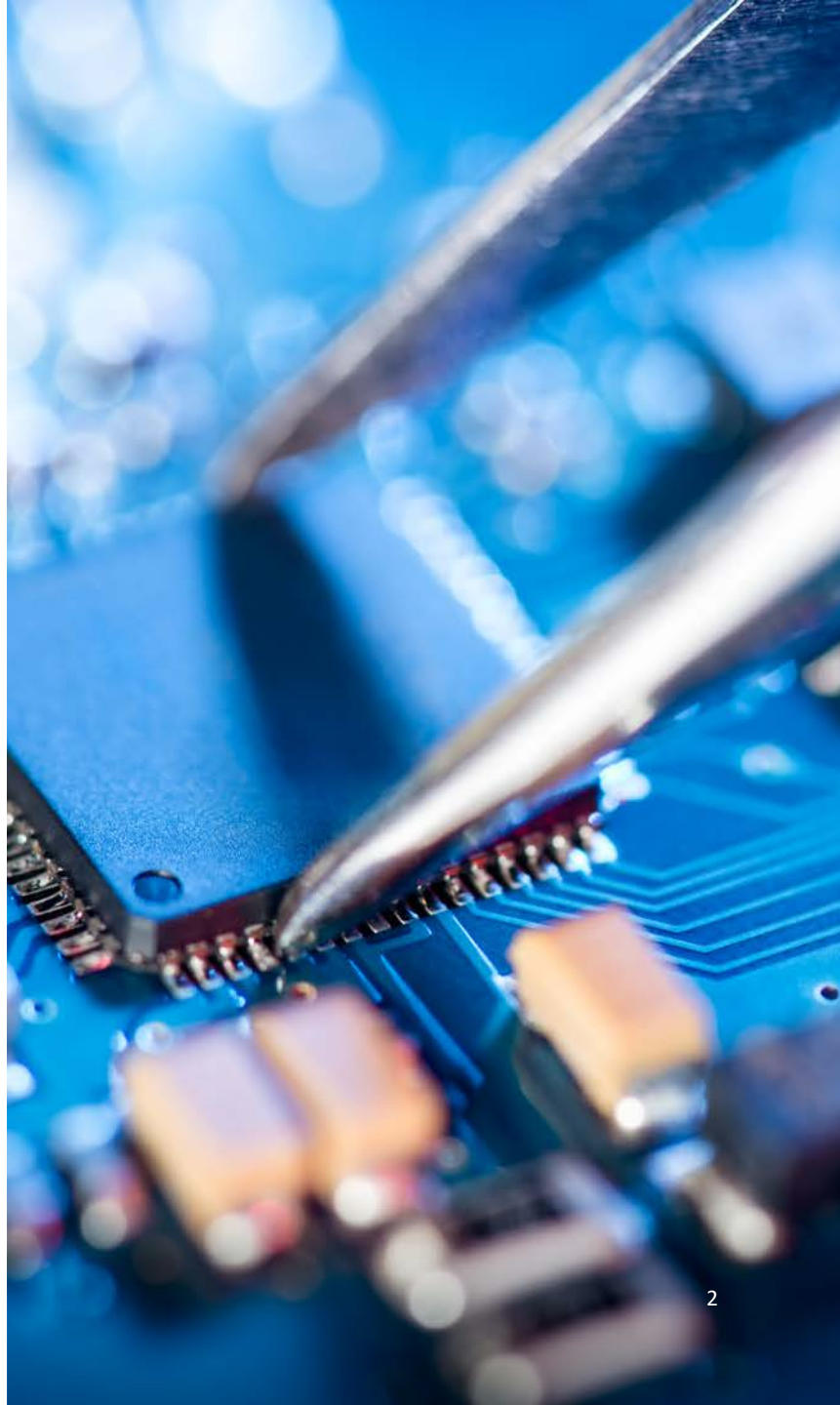
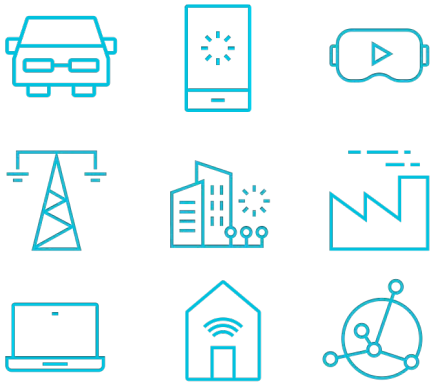
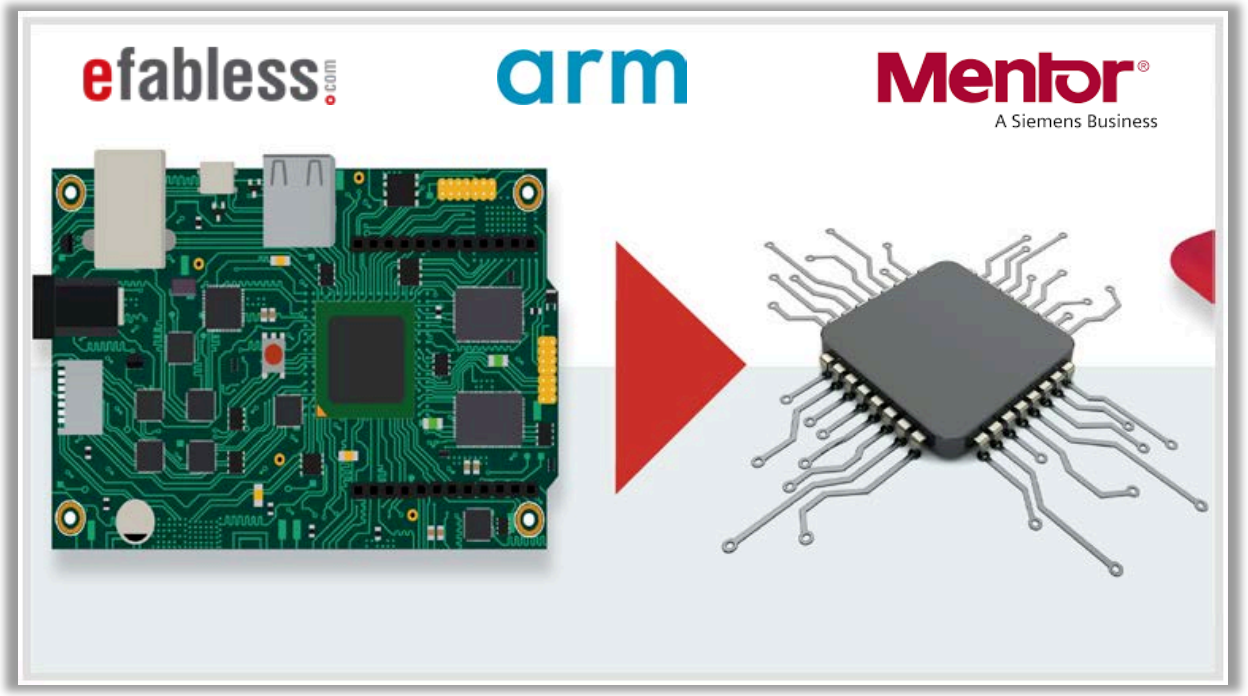
- Introduction
- Developing with SoC Design Template
- Design Implementation
- Where to Go Next

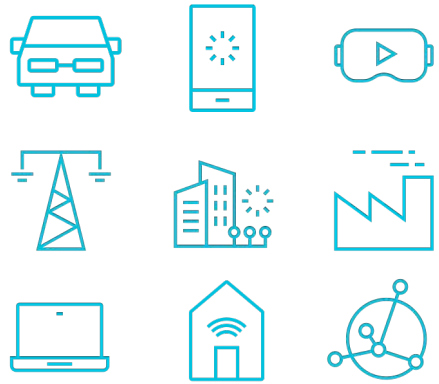


Open Innovation

Enabling 1 Trillion Connected Devices







Enabling anyone to build custom silicon

Open innovation leveraging the Arm ecosystem

Barriers to Custom SoC

Addressing those barriers will open a larger Custom SoC market

Inertia

- Standard chips "good enough"
- No simple solution

Knowledge gap

- Don’t know it’s an option
- "Space of the Possible" with Custom SoC
- Development process
- Cost NRE
- Potential unit cost
- How to source IP/tools

Capabilities gap

- Team
- Skill set
- Address book
- Ability to specify
- Ability to select the right partners

Cost

- High NRE cost
- IP licensing
- Development time

Perceived risk

- New venture out of “core competencies”
- Many unknowns
- Missing market window

Breaking Down the Barriers

Inertia

- Demonstrate capabilities
- Show success stories
- Abstract complexity

Knowledge gap

- Centralize information
- Show what can be included in SoCs
- Connect to partners that can bring knowledge in
- Bring transparency (cost, quality, user feedback)

Capabilities gap

- Easily connect to design partners
- Reference systems
- Bring elements of the supply chain in a single place

Cost

- No large upfront cost for infrastructure, IP or EDA
- Rapid design time/time to samples
- Shared knowledge and starting point

Perceived risk

- Trusted platform
- Reduce unknowns
- Predictable time to silicon samples
- Industry standard tools and IP

SoC Design Templates

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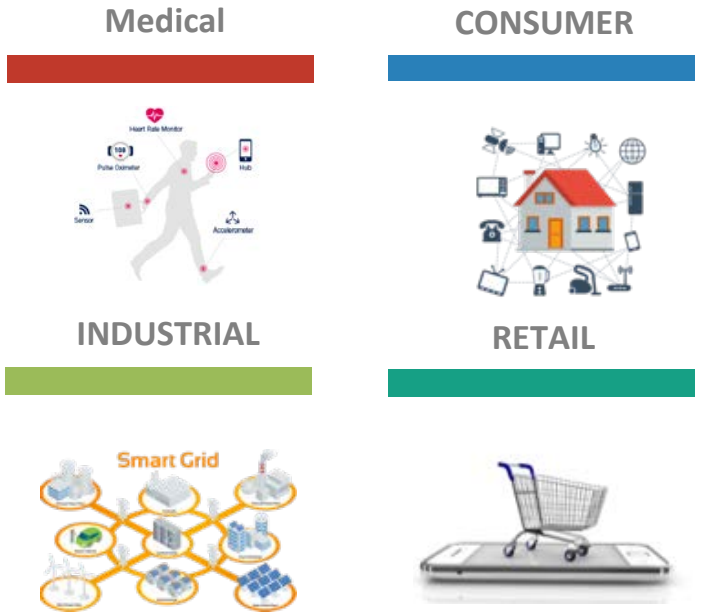
SoC Design Templates

Foundation for Open Innovation

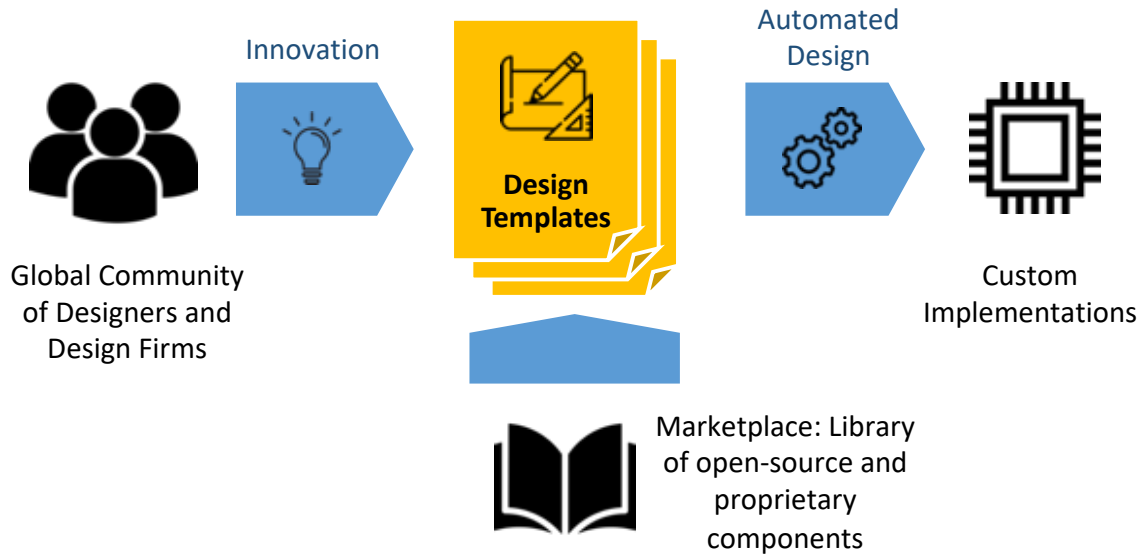
PROBLEM

Electronics are required for all products but are too complex, time consuming and expensive to create



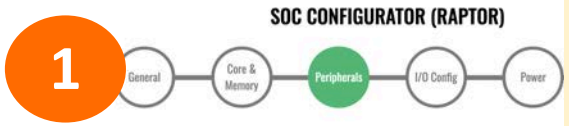
SOLUTION

A New Development Model Based on Pre-Engineered Open Source Design Templates

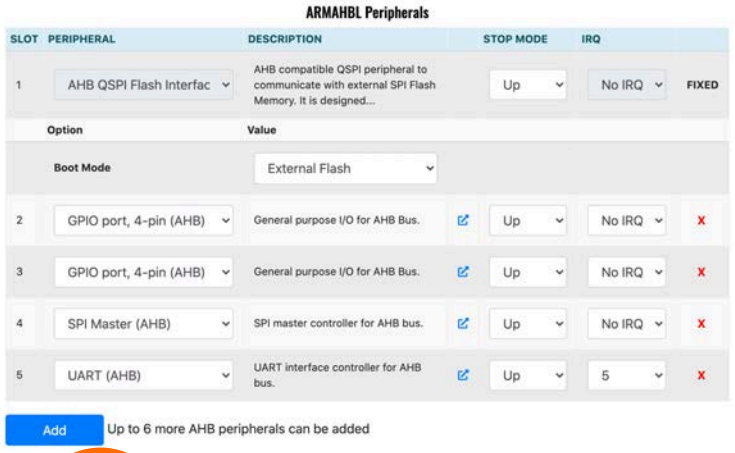


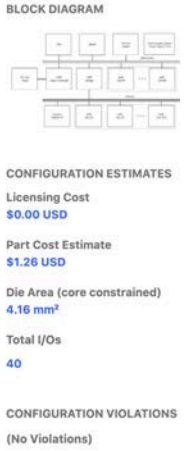
Development Flow

1



Easy web-based drop-down menu configuration





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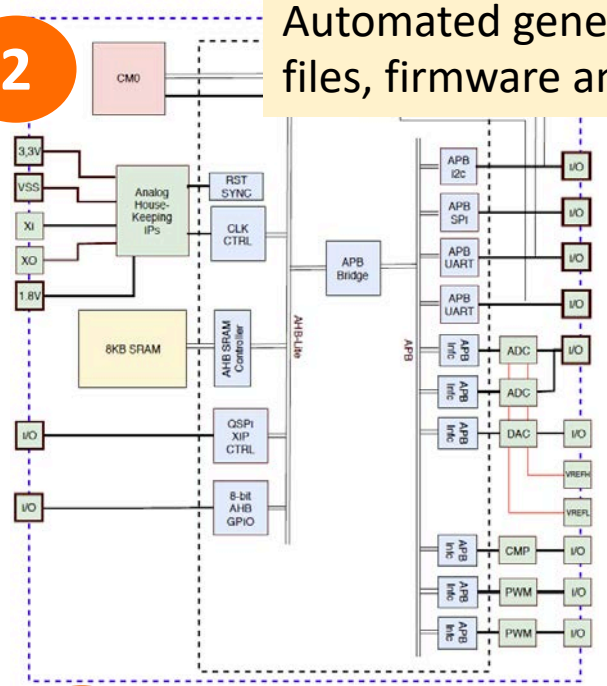
Automated generation of design files, firmware and testbenches



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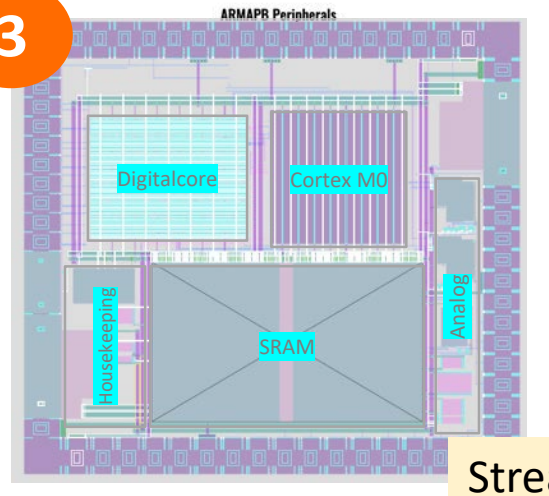

Streamlined implementation

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Fast and affordable delivery of silicon samples

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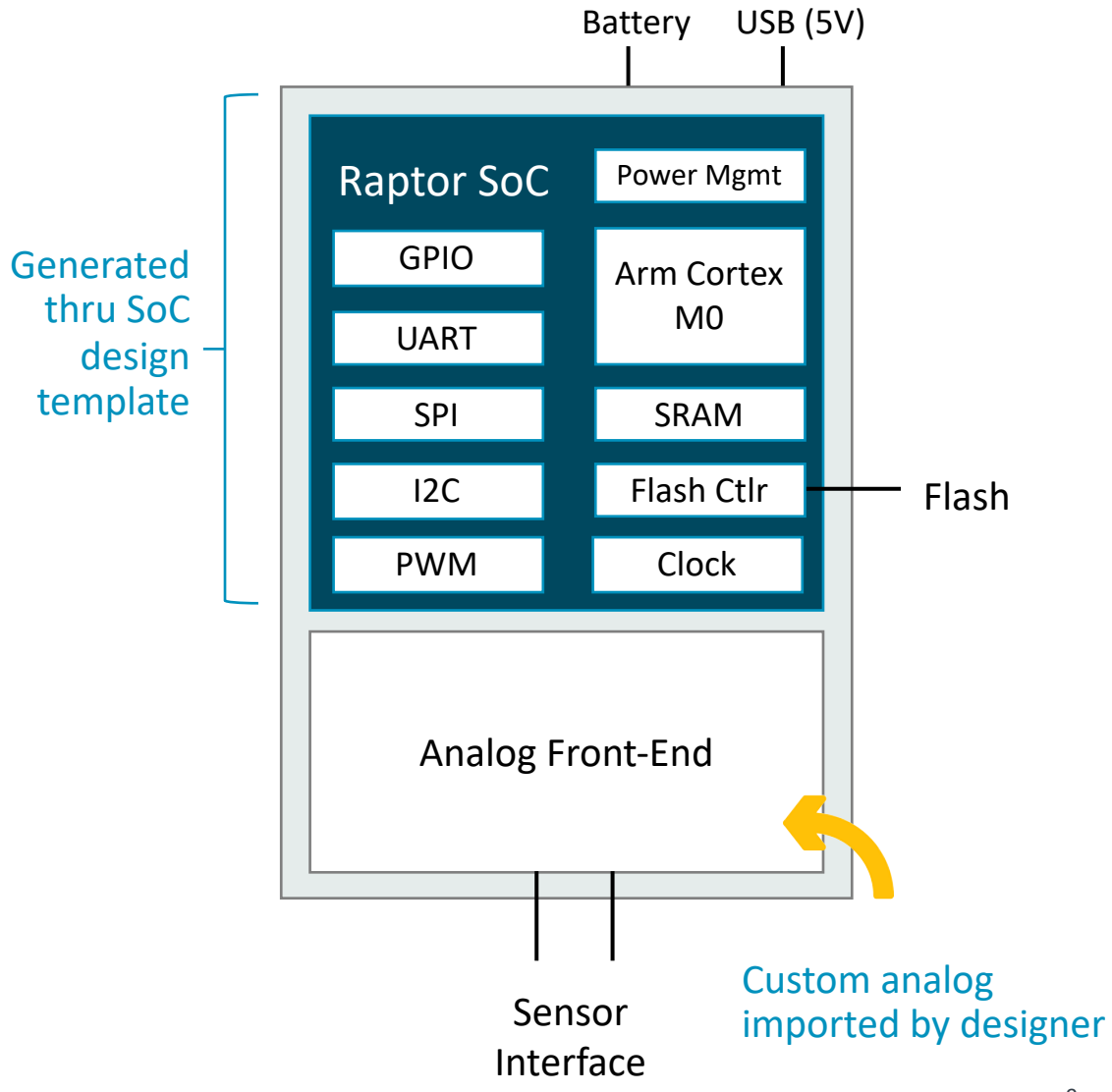
ASIC for an Intelligent MEMS Sensor

Combines custom analog front-end with configurable SoC design template

- Leverage SoC design template for MCU-based ASIC controller
- Configuration optimized based on application requirements
- Leverages existing design for digital system design
- Integrated with user provided analog front-end
- Example front-end with digital bus wrapper provided



Configuring the SoC

ARMAHBL Peripherals

SLOT	PERIPHERAL	DESCRIPTION	STOP MODE	IRQ
1	AHB QSPI Flash Interfac	AHB compatible QSPI peripheral to communicate with external SPI Flash Memory. It is designed...	Up	No IRQ
	Option	**Value**		
	Boot Mode	External Flash		
2	GPIO port, 4-pin (AHB)	General purpose I/O for AHB Bus.	Up	No IRQ
3	GPIO port, 4-pin (AHB)	General purpose I/O for AHB Bus.	Up	No IRQ
4	SPI Master (AHB)	SPI master controller for AHB bus.	Up	No IRQ
5	UART (AHB)	UART interface controller for AHB bus.	Up	5

Add Up to 6 more AHB peripherals can be added

CONFIGURATION ESTIMATES

Licensing Cost
$0.00 USD

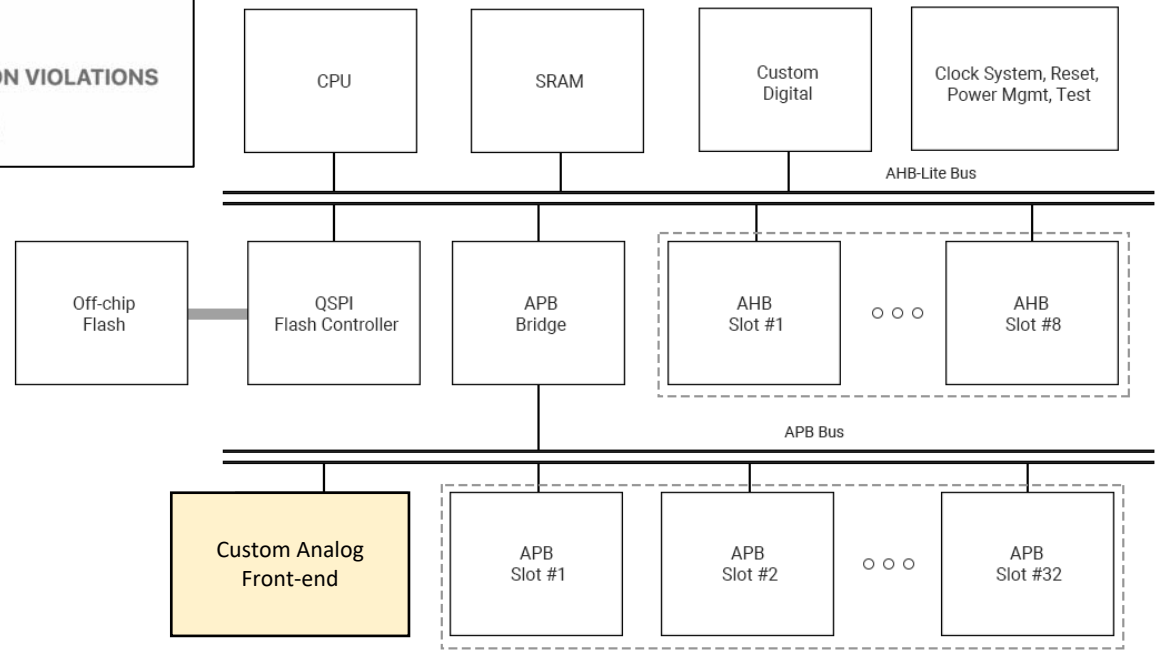
Part Cost Estimate
$1.27 USD

Die Area (core constrained)
4.21 mm²

Total I/Os
53

CONFIGURATION VIOLATIONS

(No Violations)



Saved SoC Configuration

Automated Design Generation

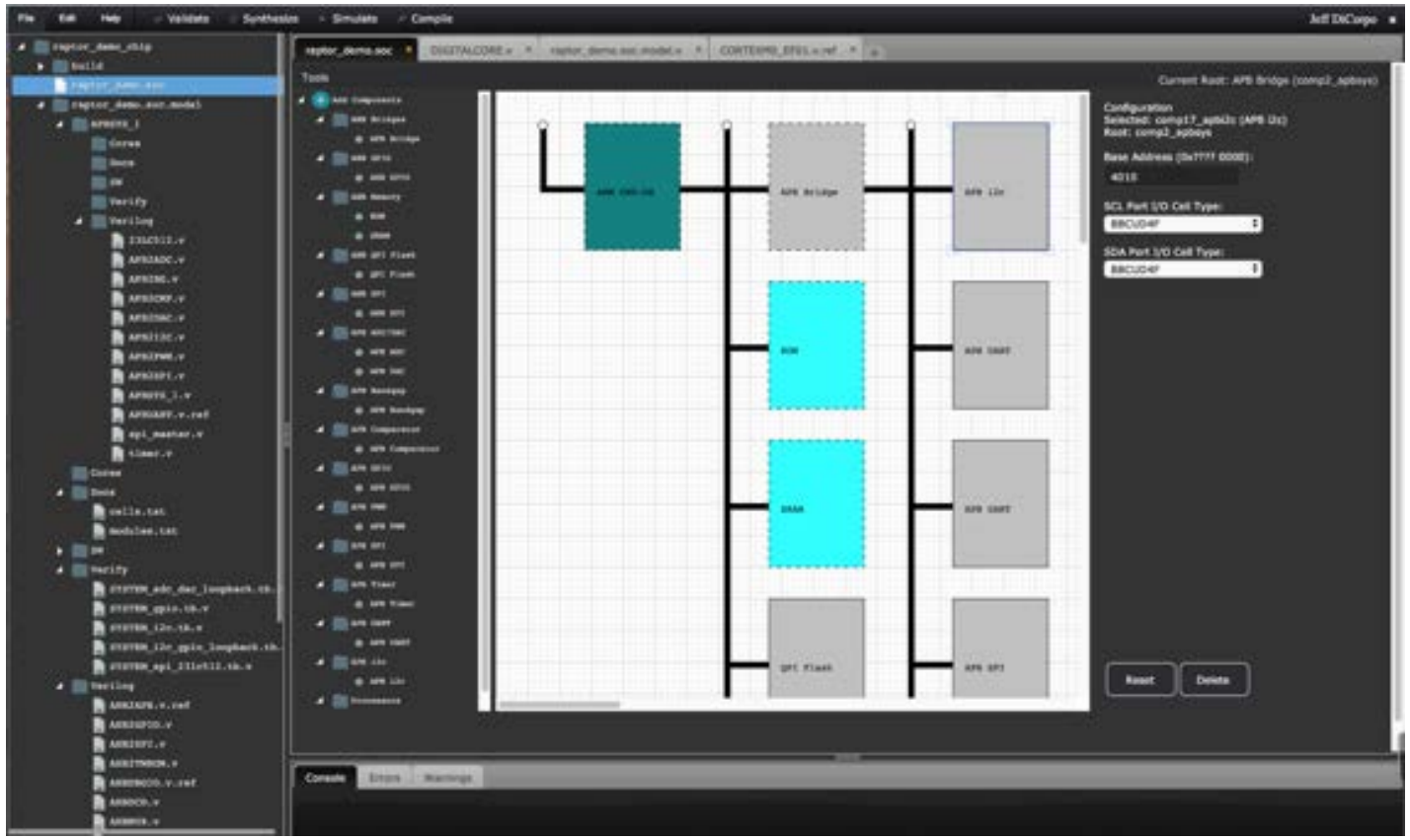
Configurations stored from web configurator

Tool automatically generates a top-level SoC model

Inspect and confirm configuration settings

SoC generator builds the set of design files:

- Top-level design
- Verilog source files
- Testbenches
- Firmware stub files



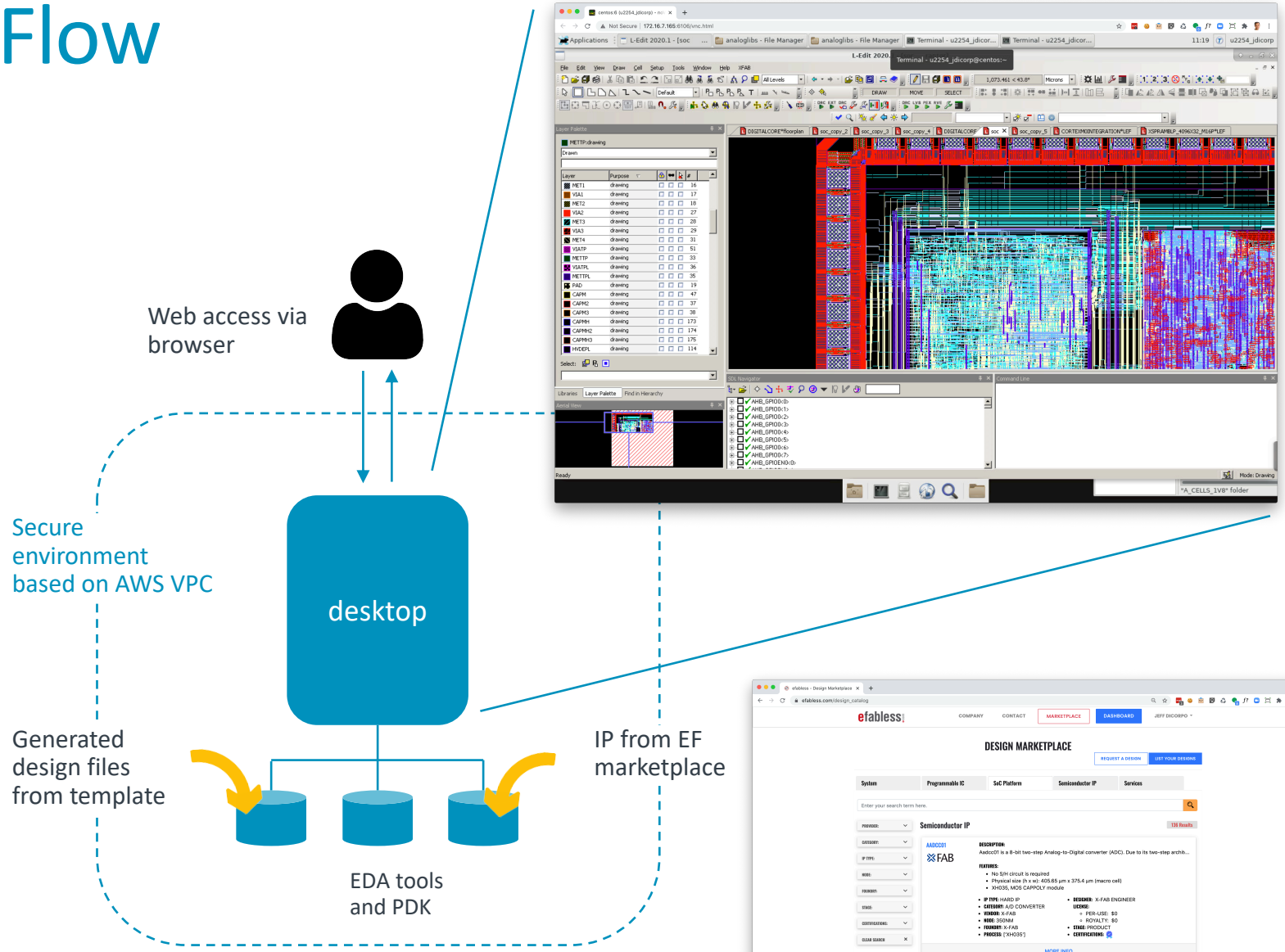
Tanner EDA Design Flow

Design files are exported to desktop with EDA design flow on the platform

- Preconfigured environment with foundry PDK
- All IP exists in the marketplace
- Design is generated to be implementation ready with the design flow

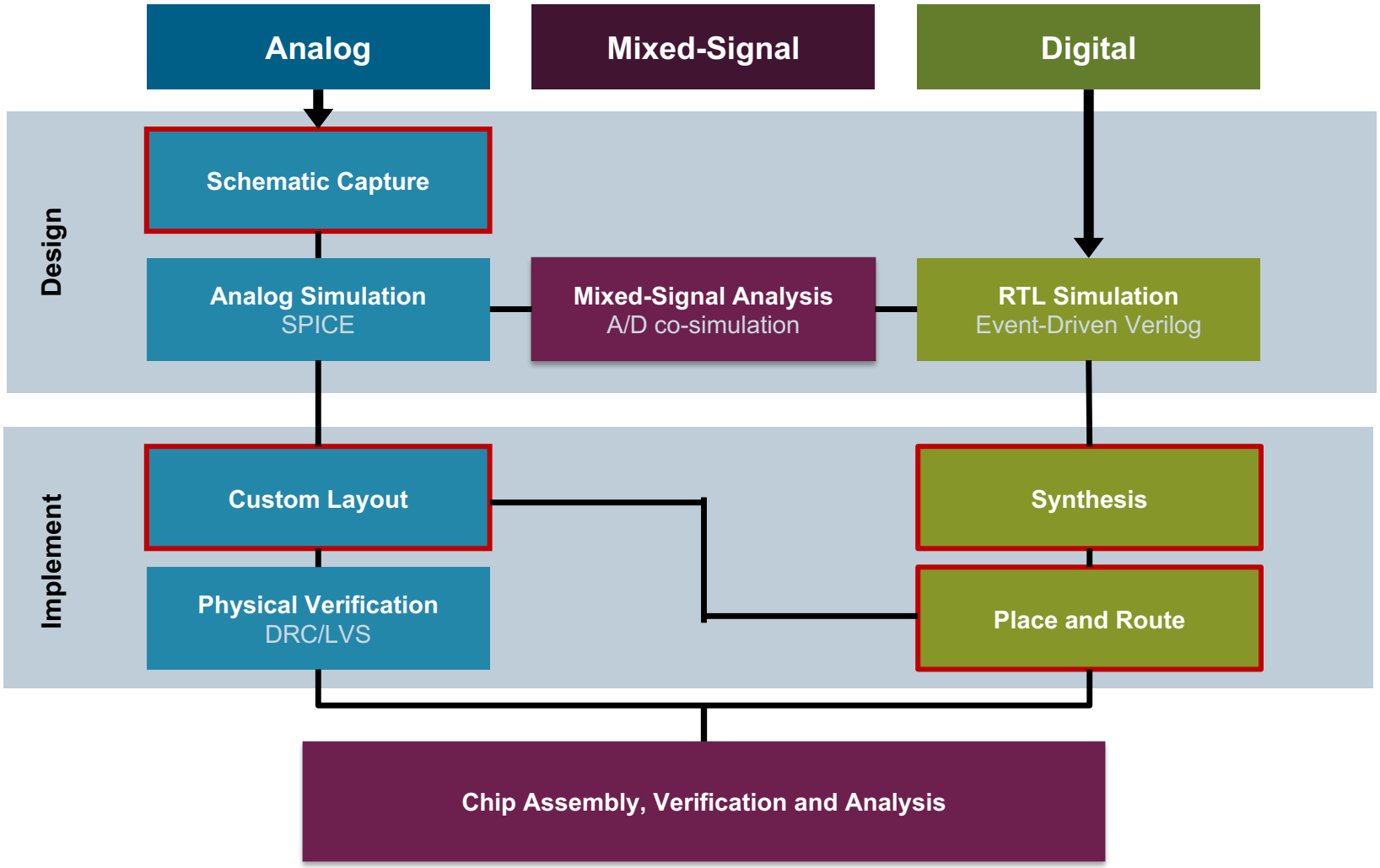
Multi-user access support

Utilize your existing licenses for Tanner EDA



Design Implementation

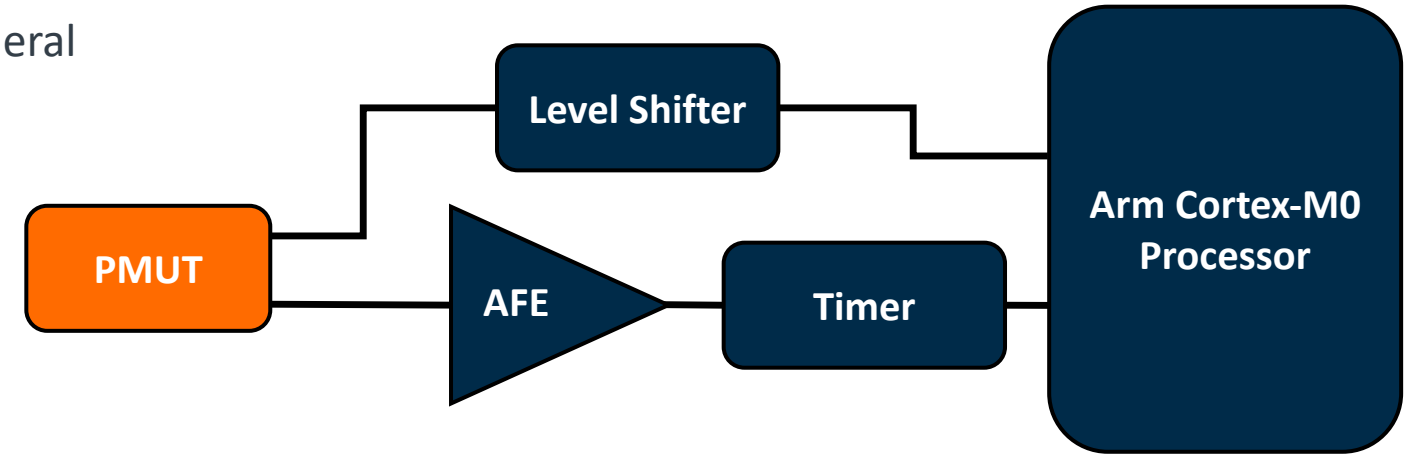
Typical Mixed Signal IC Implementation Flow



Full Custom Block Design

Active sensor requires custom analog driver and readout circuit

- Transmit pulse requires 12V drive circuit
  - Boosted from 3V control signal from µC
- Receive logic must detect 500 microvolt signal
  - RX detect signal amplified to 3V logic level and latched
- Circuit interfaces directly to APB bus
- Time of flight measured by µC using timer peripheral



Behavioral Modeling

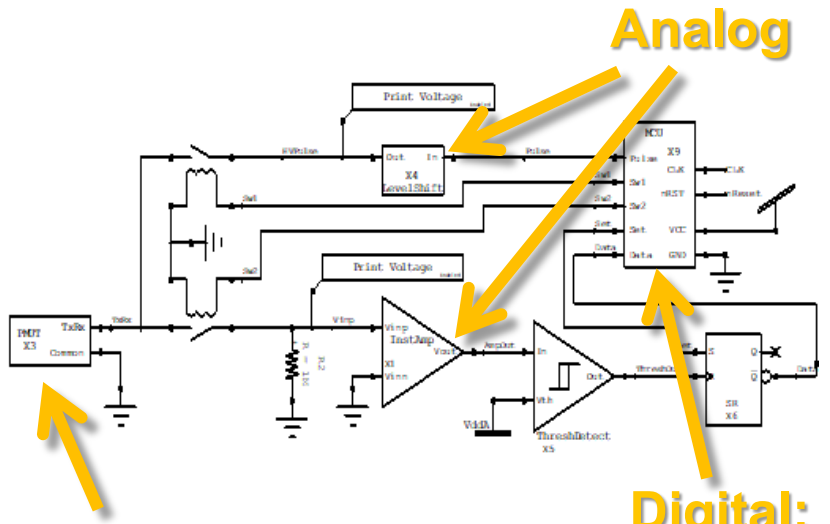
Top-down design with executable model of MEMS PMUT

Top-down model created using a combination of techniques

- Verilog-A reduced-order model for MEMS transducer
- Verilog-D model of APB interface
- Verilog-A models of analog components

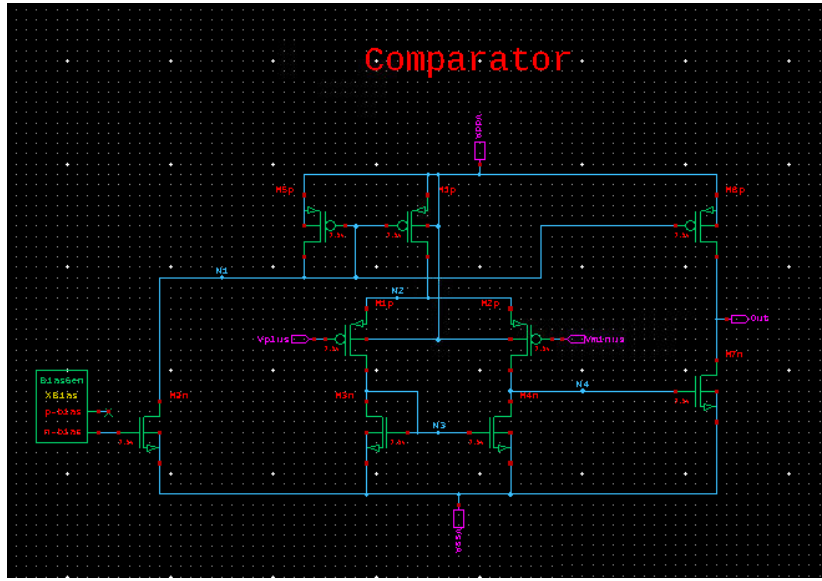
Simulated in SPICE/Verilog co-simulator

Once behavior is finalized, transistor-level design fills in analog blocks, swapping in for simulation



Analog Block Implementation

Schematic, simulation and layout

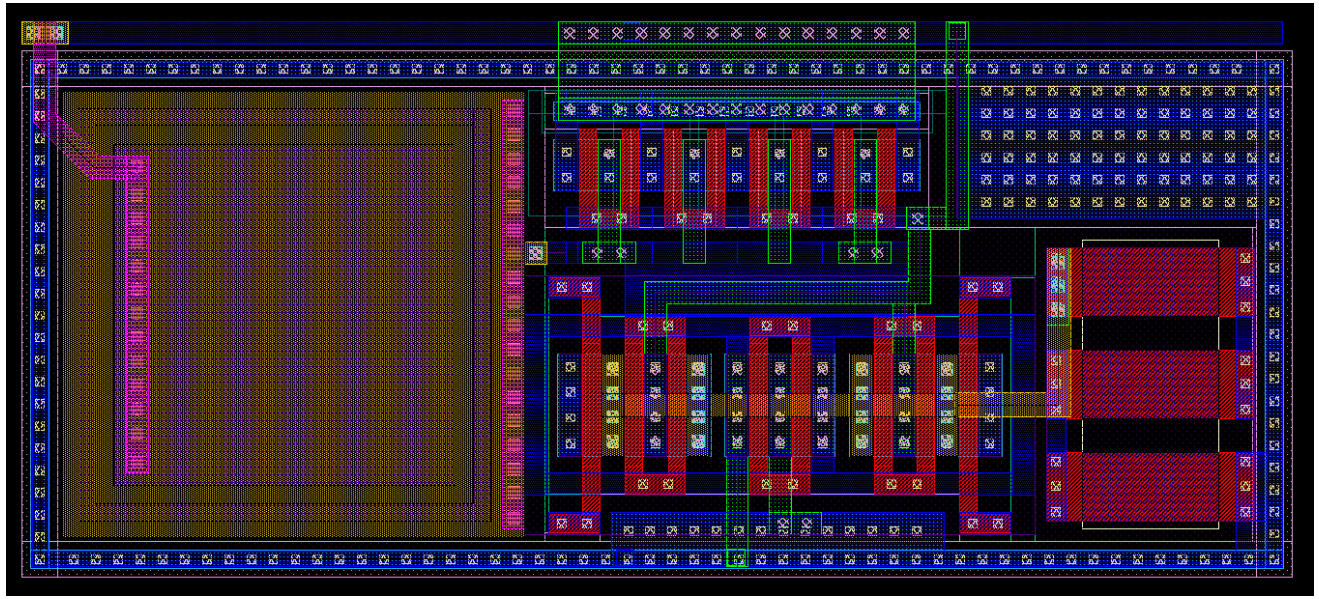


Schematic Design:

- Devices are selected from a Foundry Process Design Kit libraries based on design requirements
- Parameters are tuned for specific circuit performance
- Tight loop iteration with SPICE simulator

Custom Layout:

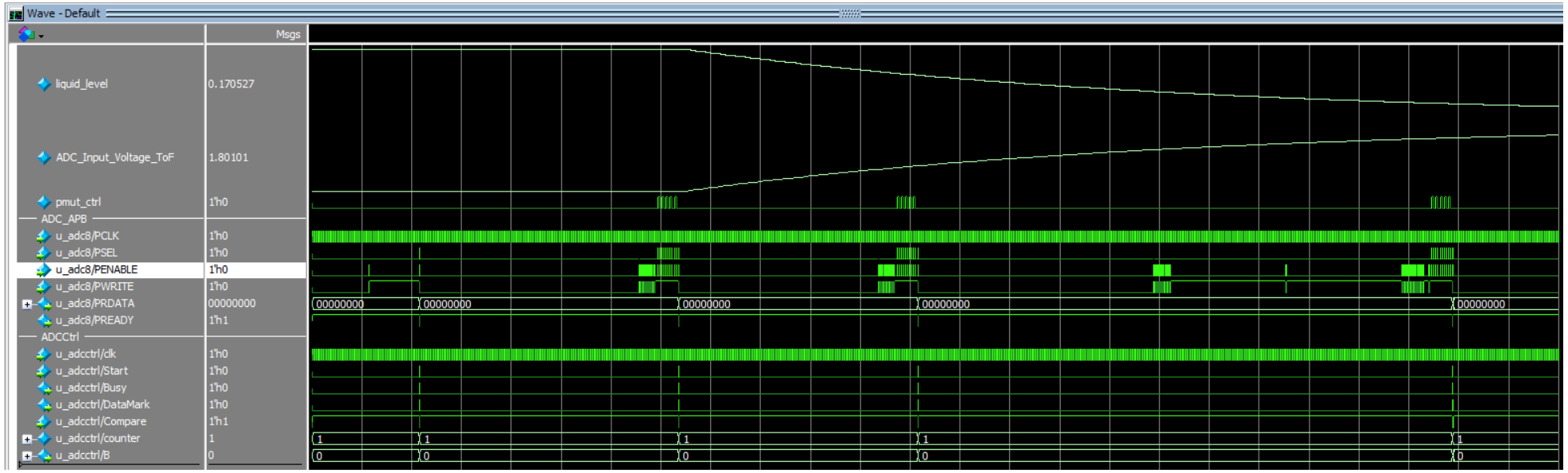
- Device layouts are automatically generated from schematic using PCells and SDL
- Layout is hand-placed and routed with care given to ensure layout effects don't compromise functionality



Top Level Simulation

Full chip simulation including RTL of major digital components

- Ensures necessary registers are exposed
- Have correct default values
- Power on and sleep/wake behavior
- System power estimation



Floorplan & Chip Assembly

Floorplan

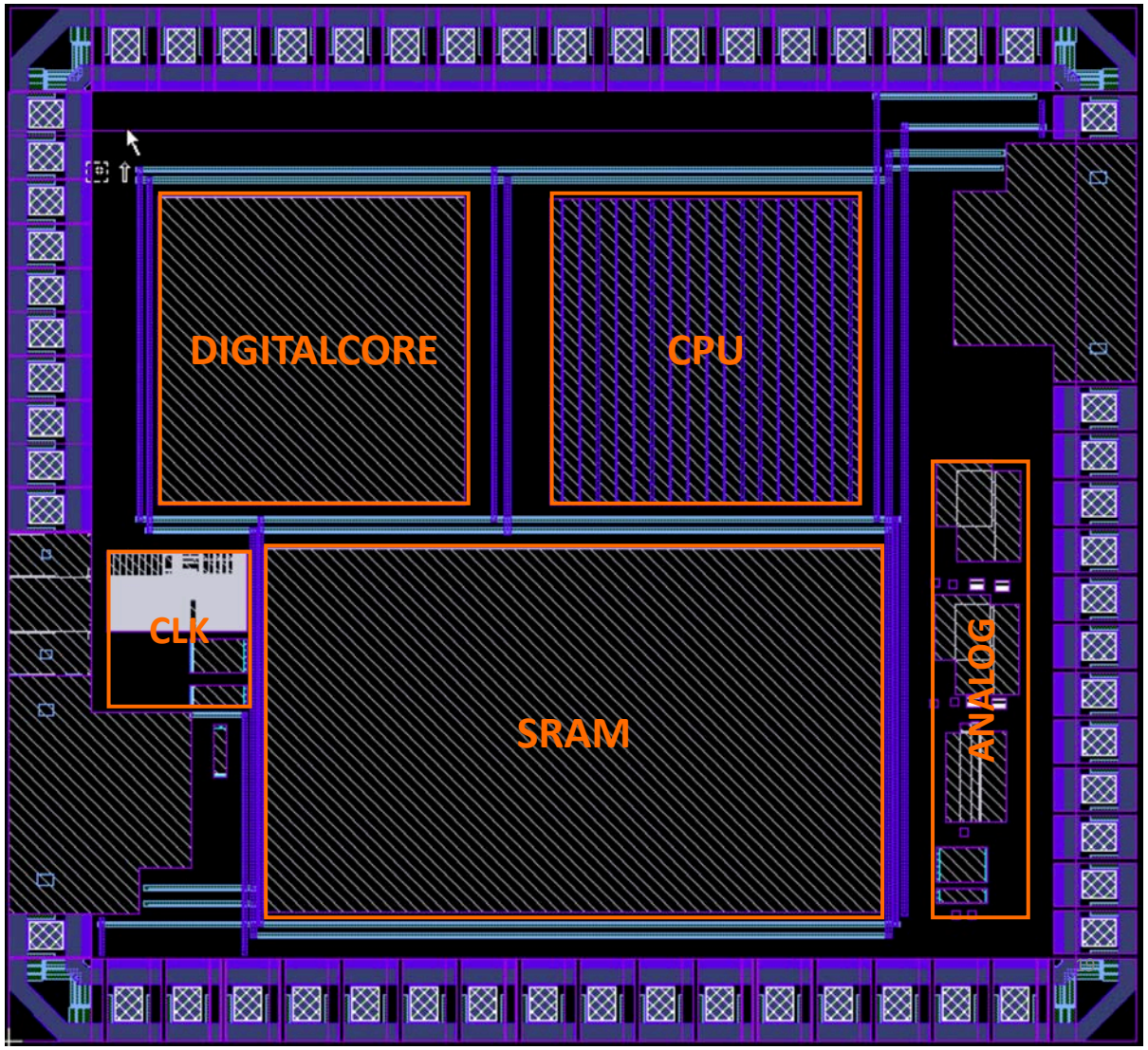
Assemble & place hard macros

Create padframe

Determine shape available for digital logic

Optimally place ports on logic periphery for connections to padframes and macros

Perform top-level power and signal routing



Digital Implementation

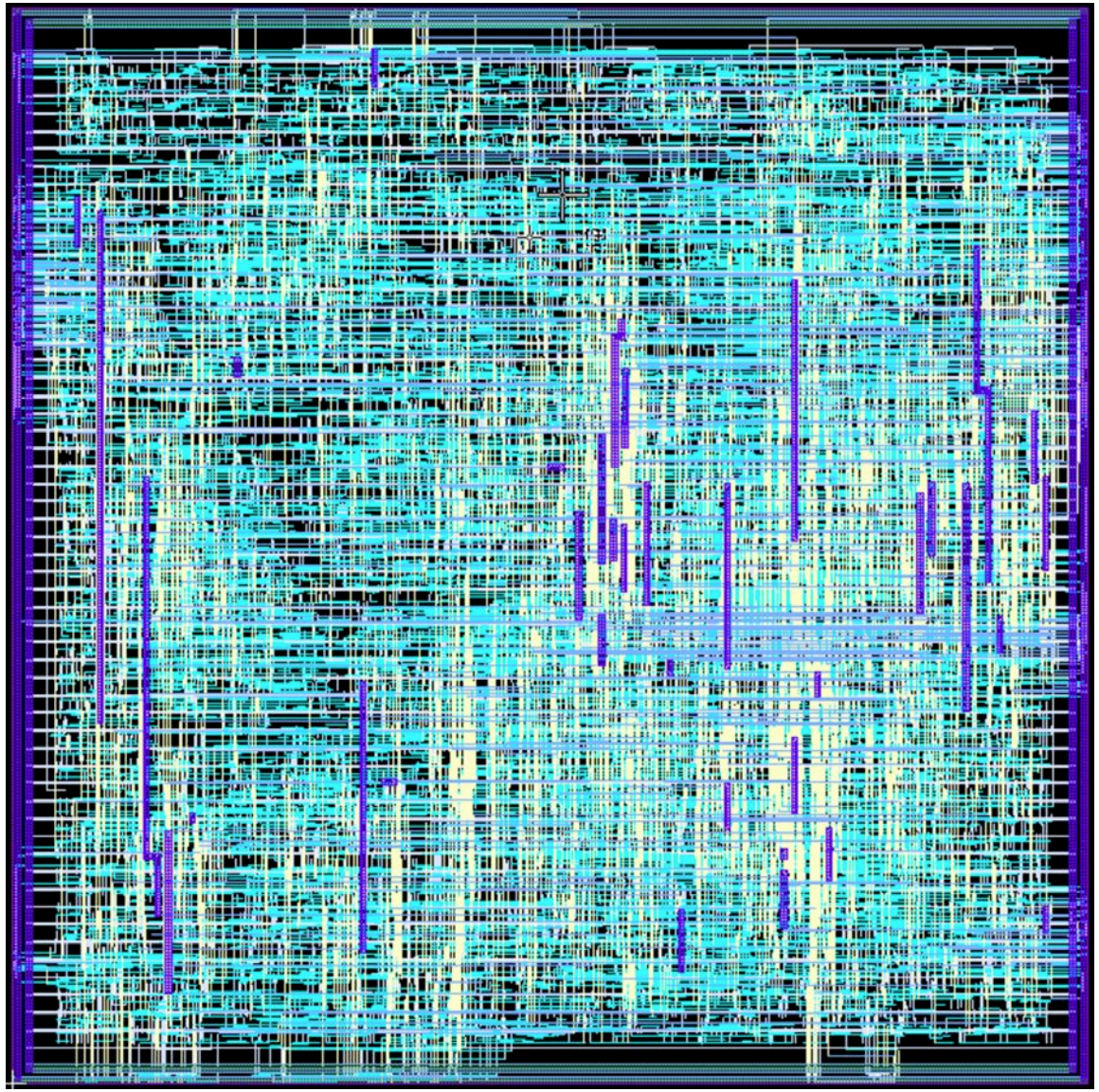
Synthesis, Placement and Routing

In contrast with analog, digital implementation is highly automated

RTL code is synthesized into a gate level netlist

P&R goes through several phases to create the design layout

- Placement and optimization
- Clock tree synthesis
- Routing
- Finalization



Verification

Physical & Circuit Verification

Design Rule Checking – make sure all shapes are manufacturable using the selected process technology

Layout vs. Schematic – make sure the all the devices are correctly sized, gates are correctly placed, and wires are all correctly connected and not shorted

Electrical Rules Checking – make sure best practices are followed regarding ESD, latchup, metal migration, etc

Functional Verification

Static and dynamic timing checks of digital logic clocking

Functional equivalency checks between design representations (RTL vs gates vs post-P&R)

System level simulations using post-layout netlists

Simulation of interconnect parasitics and layout-dependent device effects, device noise, etc

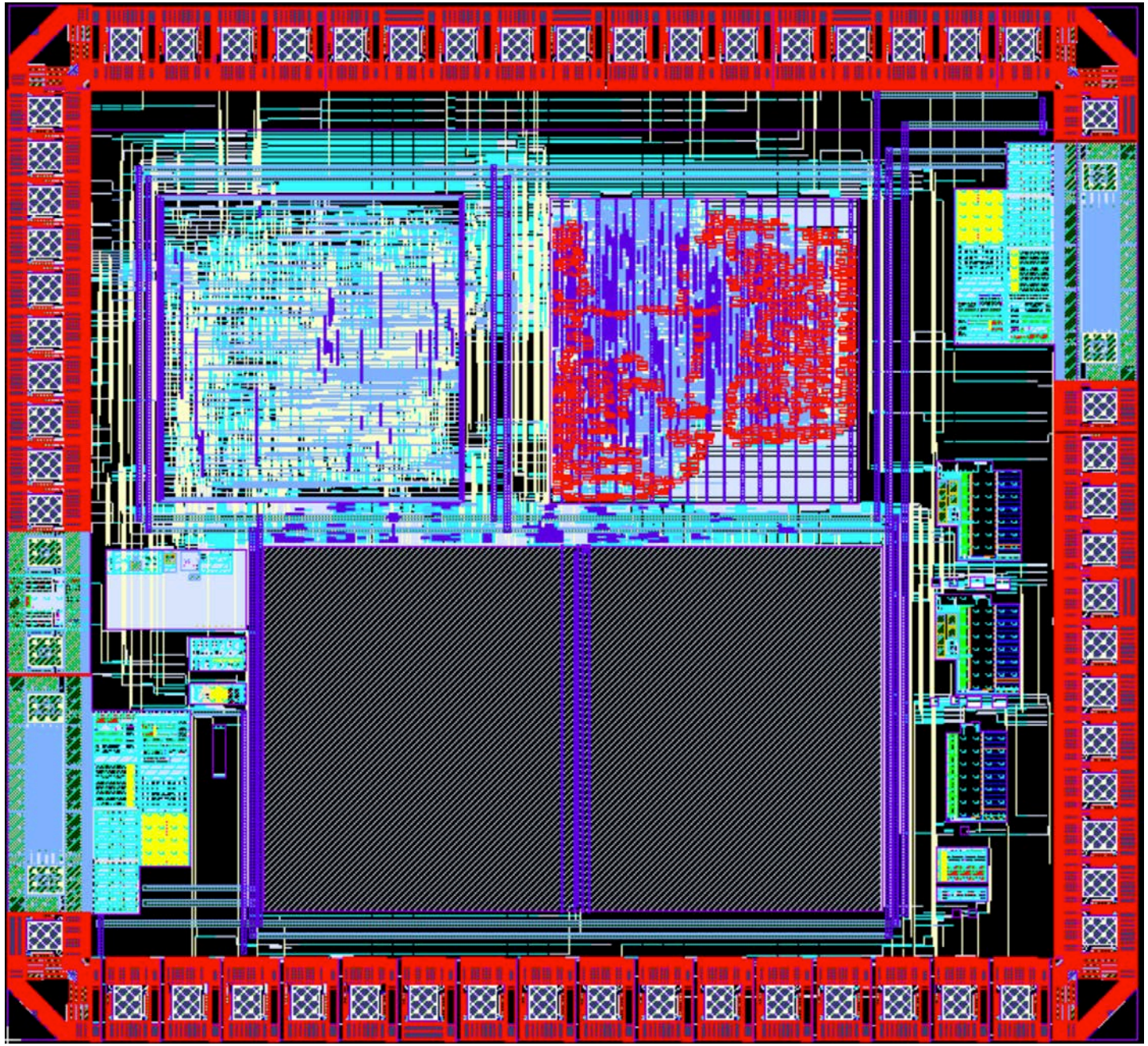
Tape-Out

Final design is sent to manufacturing

Chip finishing tasks are done like metal density fill

Final design is written to GDSII format and sent to foundry for mask-making

Foundry tape-in flow inserts black box IP like memories, repeats physical and circuit verification



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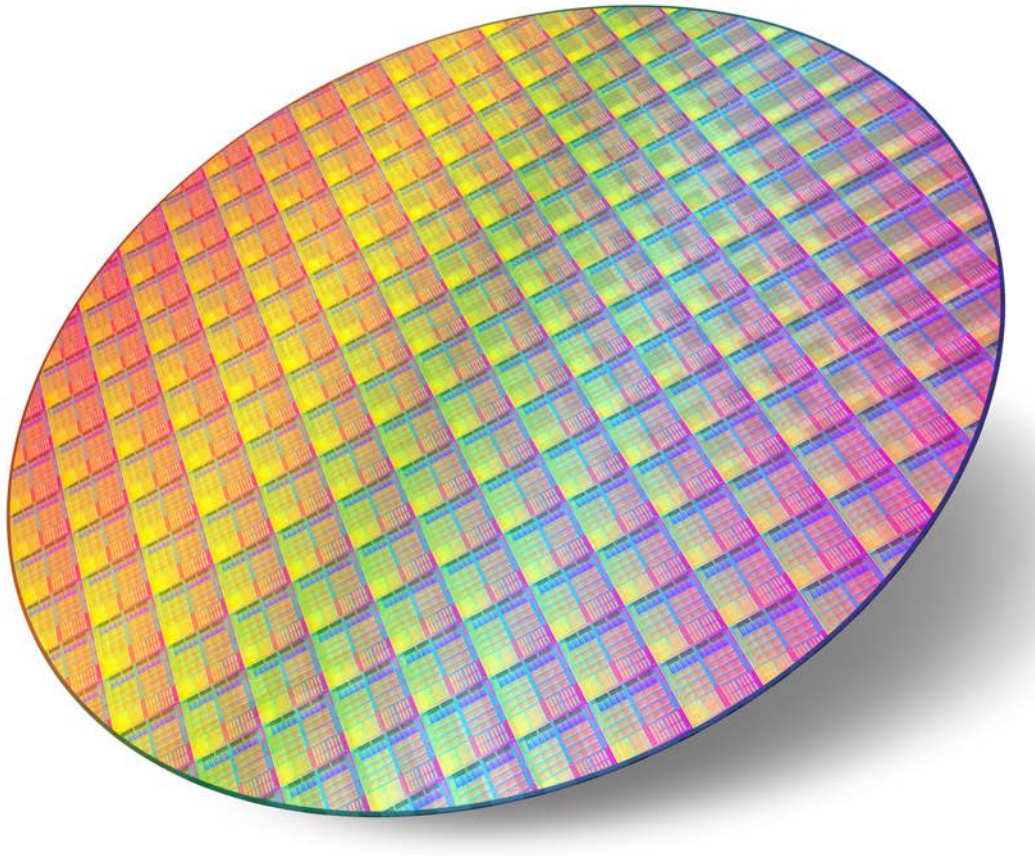
What’s Next

Fabricate Your Design

Fabrication services through the Efabless platform

- Samples starting at $26,000 for an X-FAB 180nm process node
- Packaging and PCB board options are available
- Initial volumes support
- Transition path to full-service provider for long-term support



Flexible Development Models

Choose between multiple options for development:

- **Full Turn-Key** -- full-service model
- **Design Assisted** -- physical implementation and layout
- **Roll-Your-Own** -- fabrication services only

Complete the design with Tanner EDA from Mentor

- Design on the cloud-based platform
- Bring your own license
- Upload your custom analog IP

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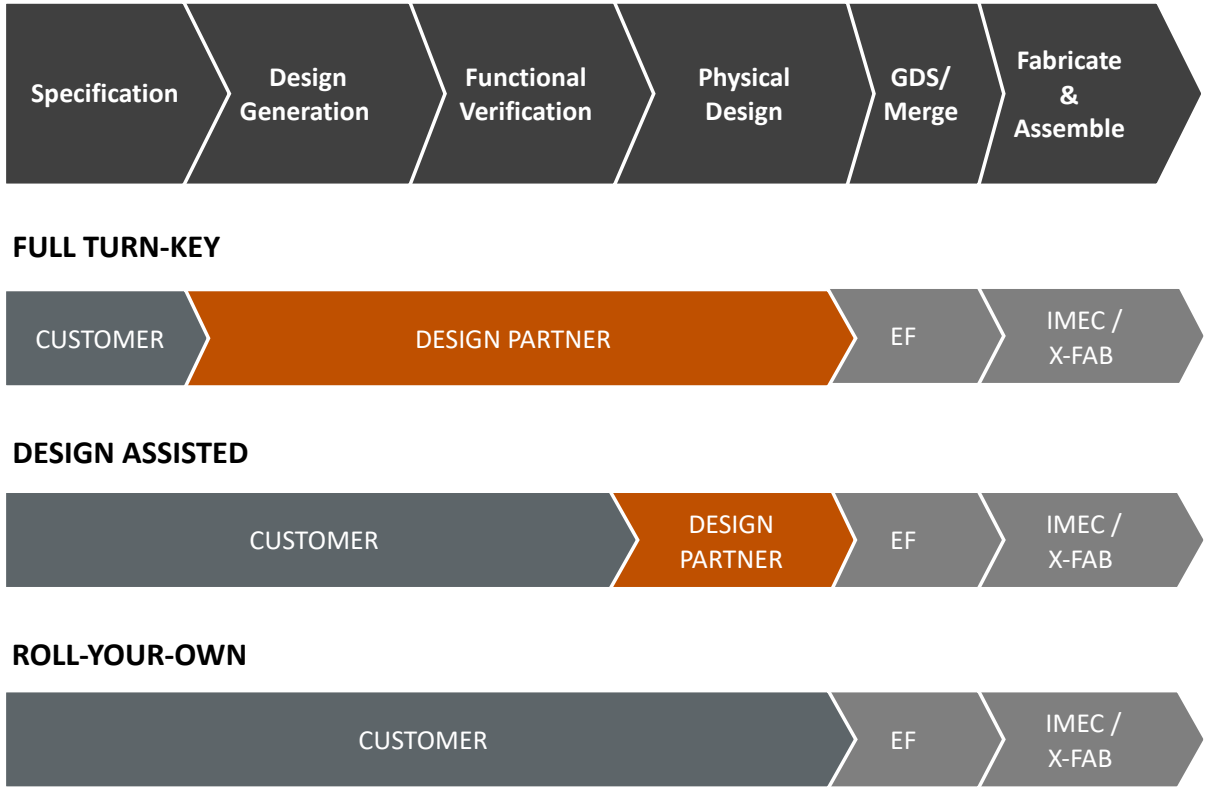


Roadmap

- new templates targeting application specific use-cases
- new IP providing more options for existing and new templates
- support for additional nodes and foundries
- support for additional Mentor / Tanner tools (e.g. RF)
- new design services and partners

Get Started !!

Go to Efabless.com and explore…

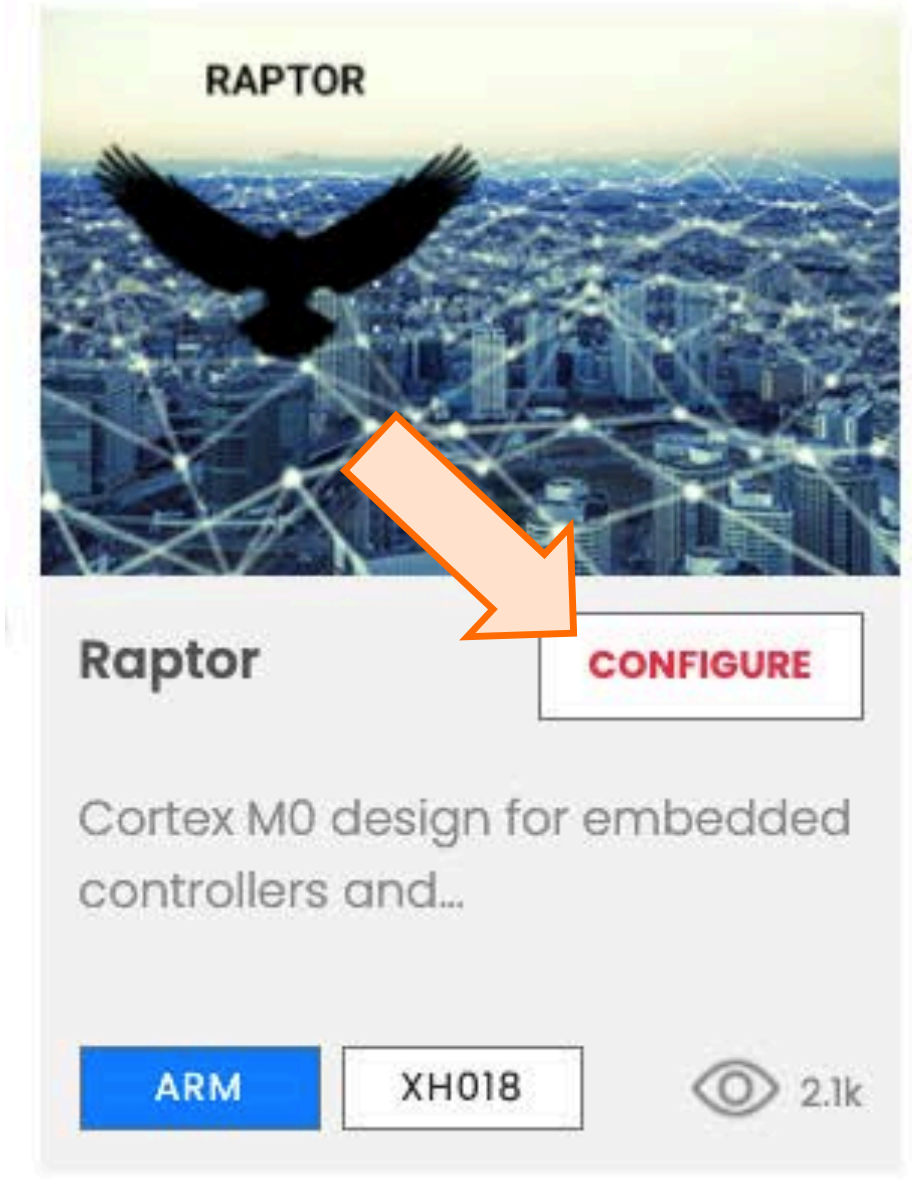
Select an SoC Template and experiment with it though the web configurator

Create a project from a saved SoC configuration and try generating the design

Contact Efabless about enabling Tanner Tools for your workspace on the platform.

Customize the design and complete the design using Mentor Tanner EDA.

Copy the SoC Templates to your own workspace on the platform and create new versions



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Thank You!

Stay up to date on the latest from Arm by checking out these developer resources: